



BENHA UNIVERSITY
FACULTY OF ENGINEERING AT SHOUBRA

Post-Graduate

ECE-606

CAD of Electronics

Lecture #3

**Design, Simulation and
Synthesize Tool Example**

Instructor:

Dr. Ahmad El-Banna



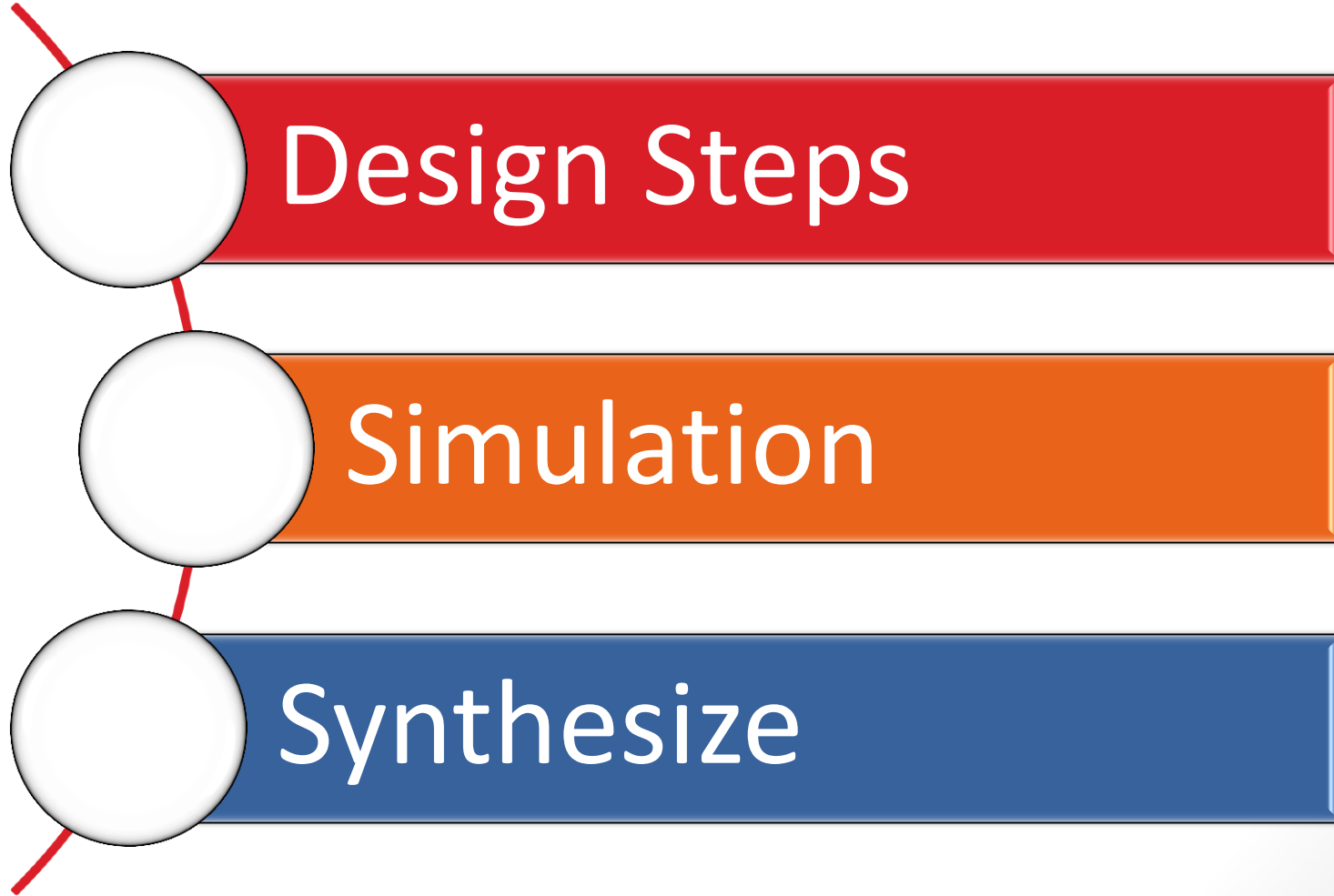
كلية الهندسة بشبرا

DECEMBER 2014

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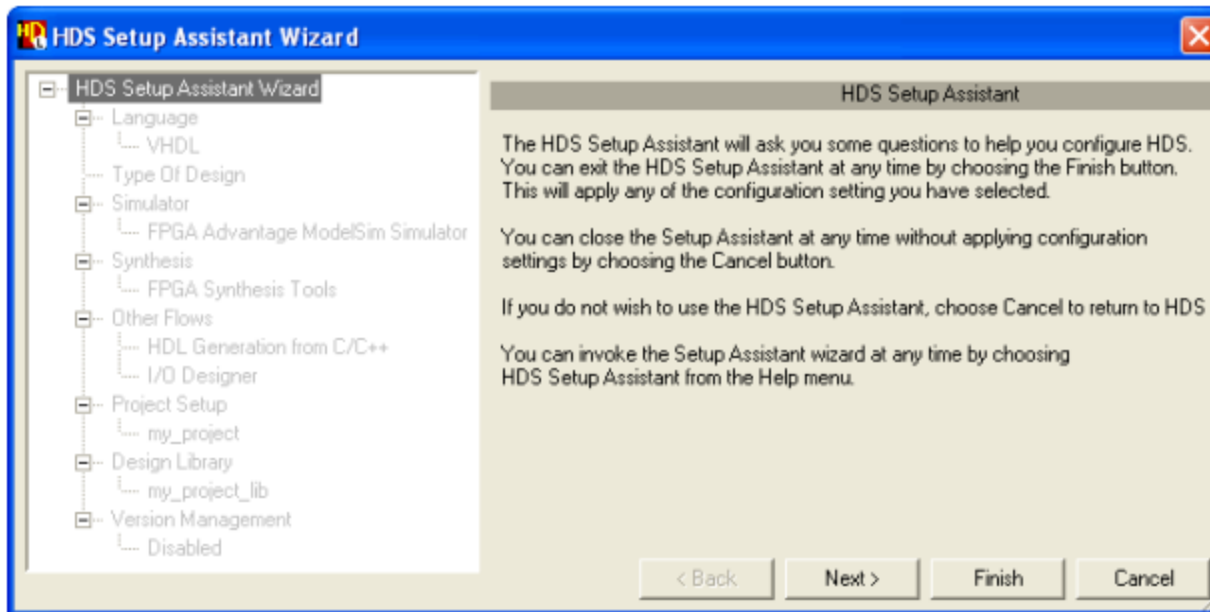
Agenda

Lecture & Lab



Invoking the Wizard

You can invoke the wizard at any time by choosing **HDS Setup Assistant** from the **Help** menu in the Design Manager window.

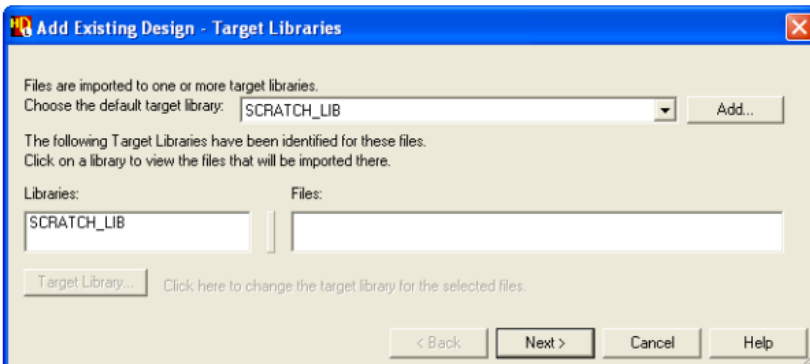
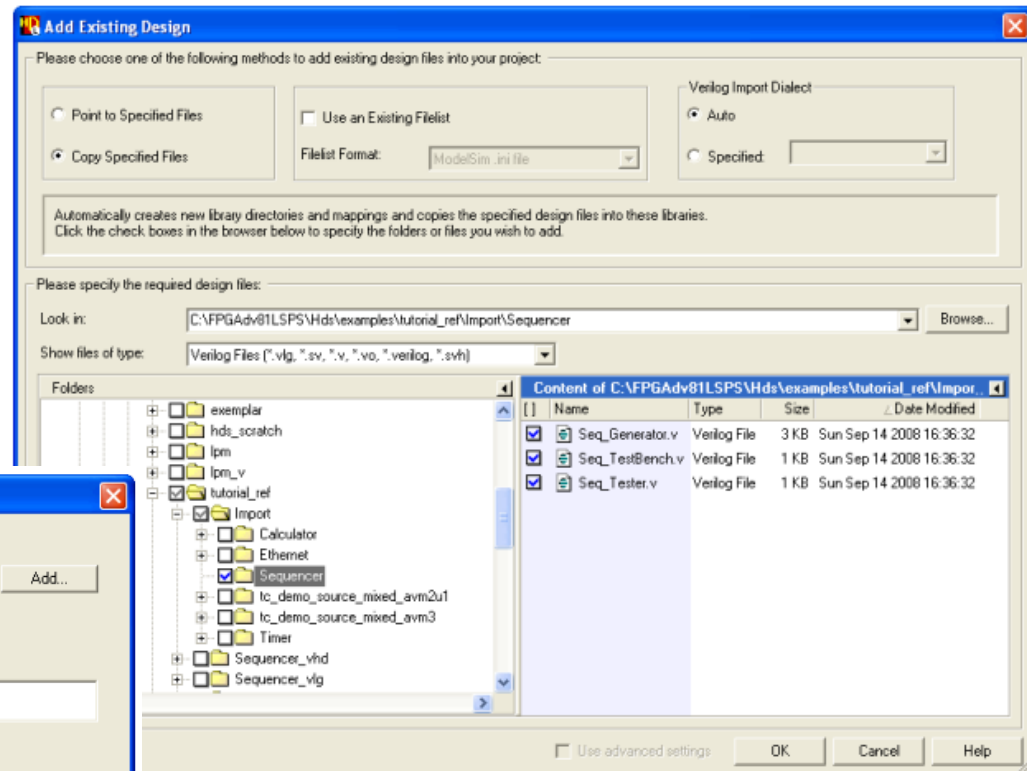


The Design Manager



Import Design

1. Choose **File> Add> Existing Design**.
2. Specify the method to add your design by selecting the *Copy Specified Files* option.
3. In the *Folders* pane, browse to the Fibonacci sequencer source code in the *examples* sub-directory of your FPGA Advantage installation. For example, if FPGA Advantage has been installed in the directory *C:\FPGAAdv81LSPS*, the path to locate the tutorial source files would be:
C:\FPGAAdv81LSPS\Hds\examples\tutorial_ref\ImportSequencer
4. From the *Show files of type* list box select *Verilog Files*.



Browse a design

Design Manager - Project examples

File Edit View HDL Tasks Tools Options Window Help

Main

New / Add

Check

Simulate

Synthesize

Document & Visualize

Explore

Tasks

Viewpoints

Design Explorer [Using viewpoint : Default Viewpoint (Filtered) - Dont Touc...]

Design Unit	Type	Extends	Language	Time Stamp
SCRATCH_LIB				
accumulator	Module		Verilog '95	Mon Sep 29 :
control	Module		Verilog '95	Mon Sep 29 :
fibgen	Module		Verilog '95	Mon Sep 29 :
fibgen_tb	Module		Verilog '95	Mon Sep 29 :
fibgen_tester	Module		Verilog '95	Mon Sep 29 :


Files

Files	Type	Extends	Size
DesignChecker			
Documentation & Visualization			
HTML			
Visualization			
SCRATCH_LIB			
accumulator	Module		
flow	Flow Chart		34 KB
control	Module		
fsm	State Machine		43 KB
fibgen	Module		
struct	Block Diagram		60 KB
fibgen_tb	Module		
struct	Block Diagram		33 KB
fibgen_tester	Module		
flow	Flow Chart		38 KB

Project SCRATCH_LIB

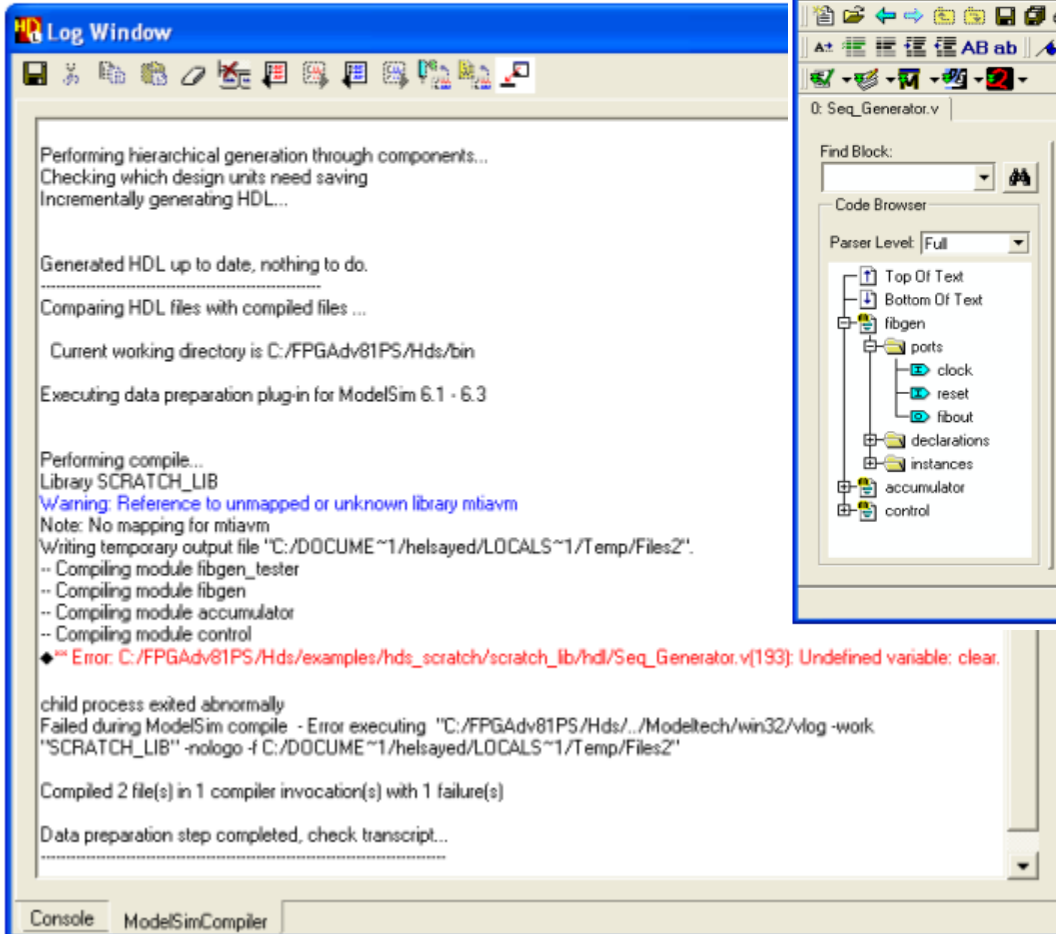


Use Model SIM to debug the design

1. Select the component design unit icon  for *fibgen_tb* in the design manager.
2. Click the **ModelSim Flow** button in the design manager toolbar.

FPGA Advantage attempts to run the ModelSim flow but HDL compilation fails due to deliberate errors in the design example source code.

The compilation status is displayed in the **Log Window**:



The Log Window displays the following text:

```
Performing hierarchical generation through components...
Checking which design units need saving
Incrementally generating HDL...

Generated HDL up to date, nothing to do.
Comparing HDL files with compiled files ...

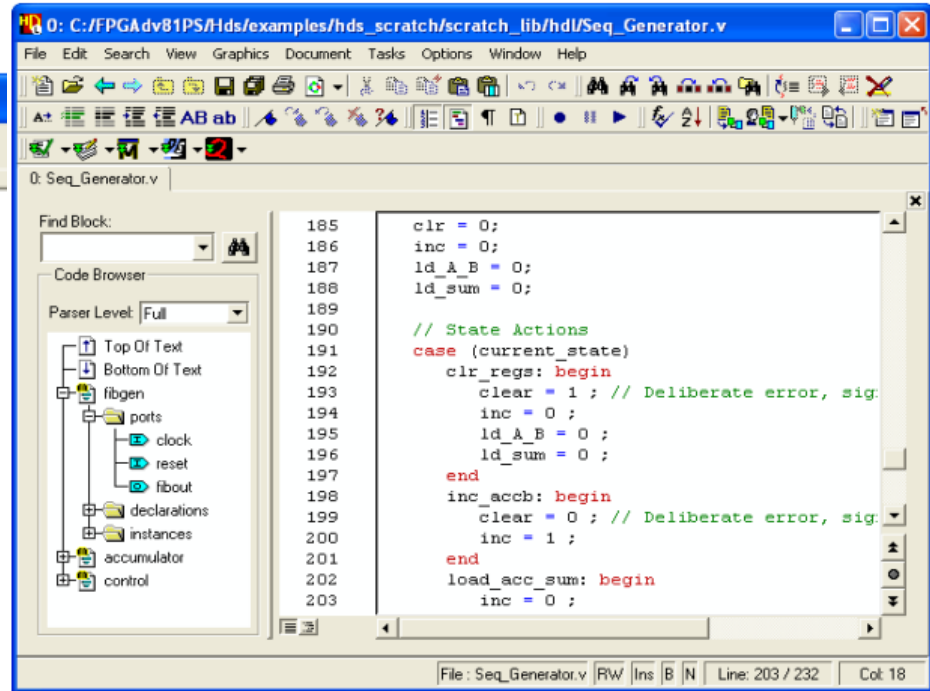
Current working directory is C:/FPGAAdv81PS/Hds/bin
Executing data preparation plug-in for ModelSim 6.1 - 6.3

Performing compile...
Library SCRATCH_LIB
Warning: Reference to unmapped or unknown library mtiavm
Note: No mapping for mtiavm
Writing temporary output file "C:/DOCUME~1/helsayed/LOCALS~1/Temp/Files2".
-- Compiling module fibgen_tester
-- Compiling module fibgen
-- Compiling module accumulator
-- Compiling module control
*** Error: C:/FPGAAdv81PS/Hds/examples/hds_scratch/scratch_lib/hdl/Seq_Generator.v(193): Undefined variable: clear.

child process exited abnormally
Failed during ModelSim compile - Error executing "C:/FPGAAdv81PS/Hds/./Modeltech/win32/vlog -work
"SCRATCH_LIB" -nologo -f C:/DOCUME~1/helsayed/LOCALS~1/Temp/Files2"

Compiled 2 file(s) in 1 compiler invocation(s) with 1 failure(s)

Data preparation step completed, check transcript...
```

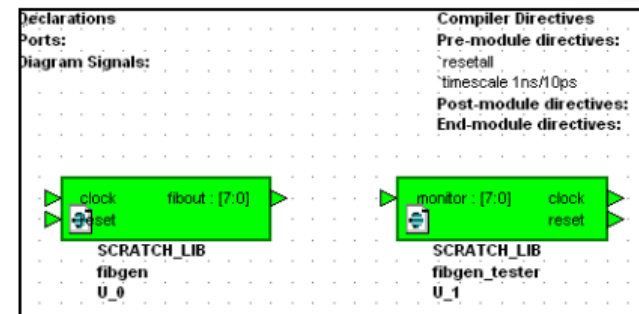
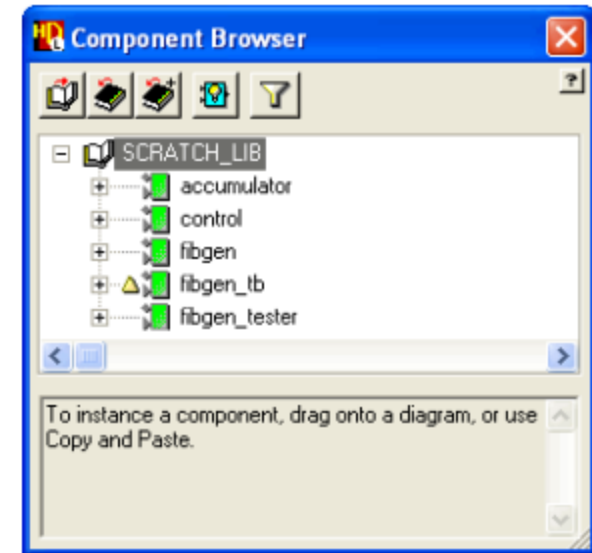
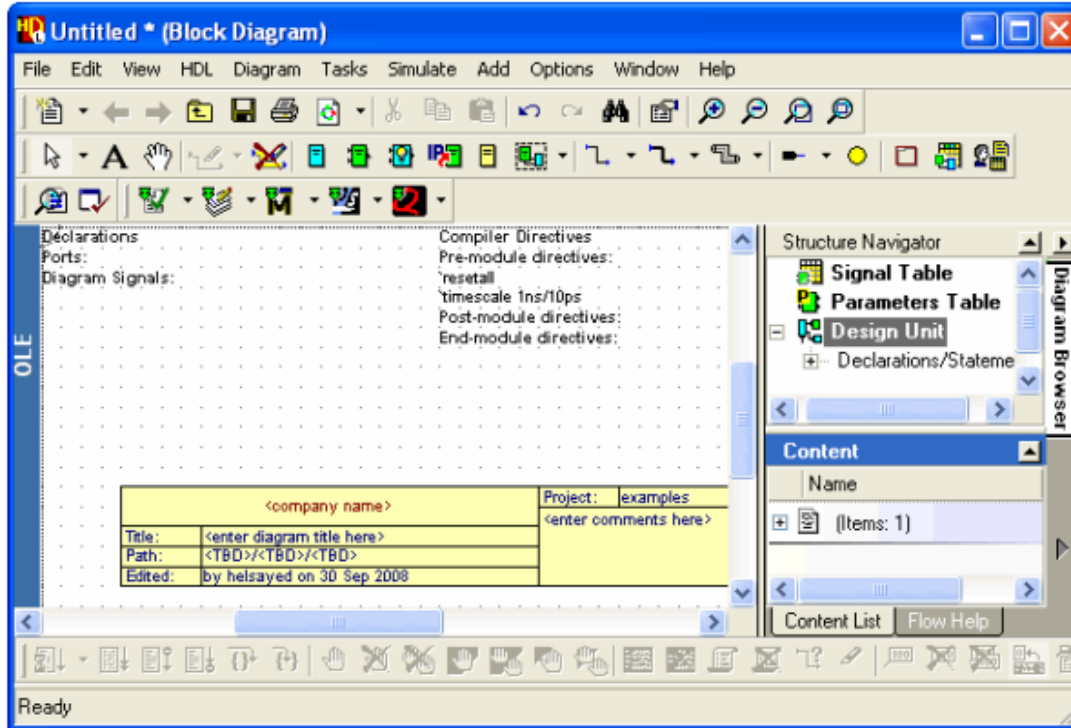


The code editor shows the following code snippet:

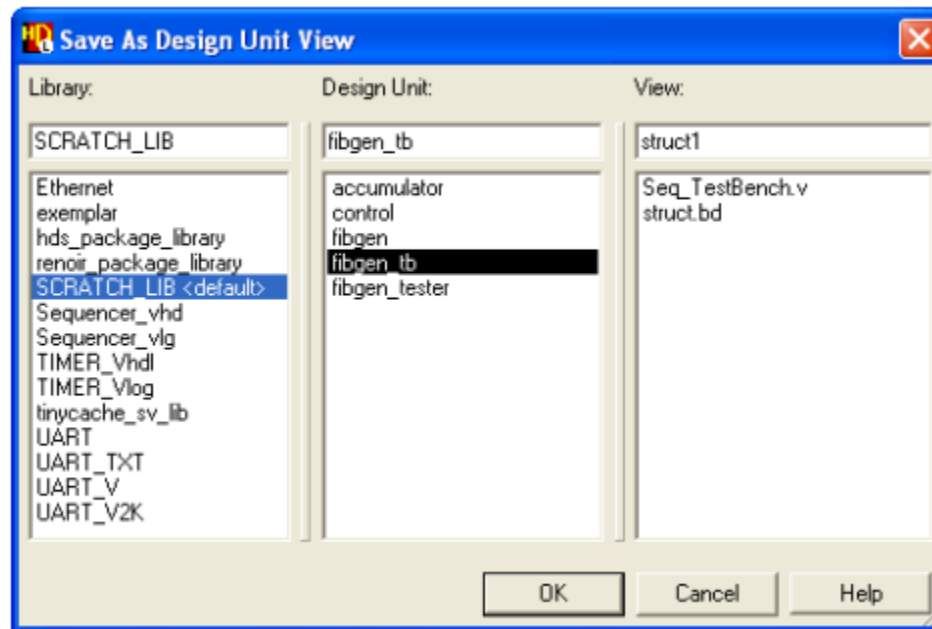
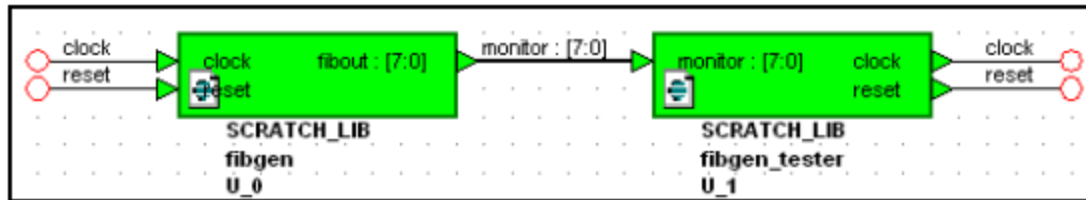
```
185
186
187
188
189
190
191 // State Actions
192 case (current_state)
193   clr_regs: begin
194     clear = 1 ; // Deliberate error, sig
195     inc = 0 ;
196     ld_A_B = 0 ;
197     ld_sum = 0 ;
198   end
199   inc_accb: begin
200     clear = 0 ; // Deliberate error, sig
201     inc = 1 ;
202   end
203   load_acc_sum: begin
204     inc = 0 ;
```


Create a graphical test bench

1. Use the **New** button in the design manager window and select **Block Diagram** from the **Graphical View** cascade of the dropdown menu to create a new untitled block diagram.



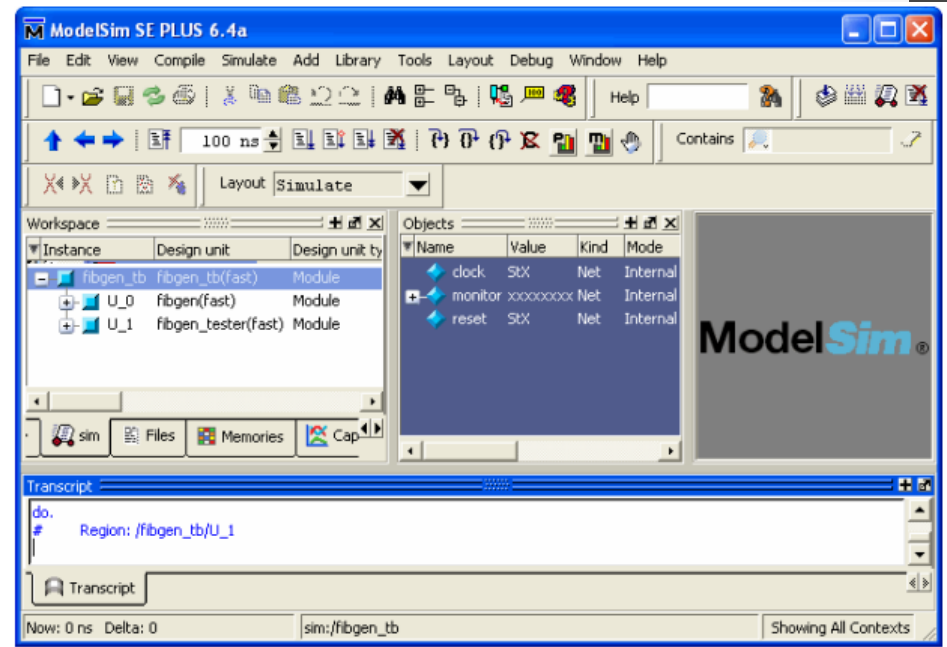
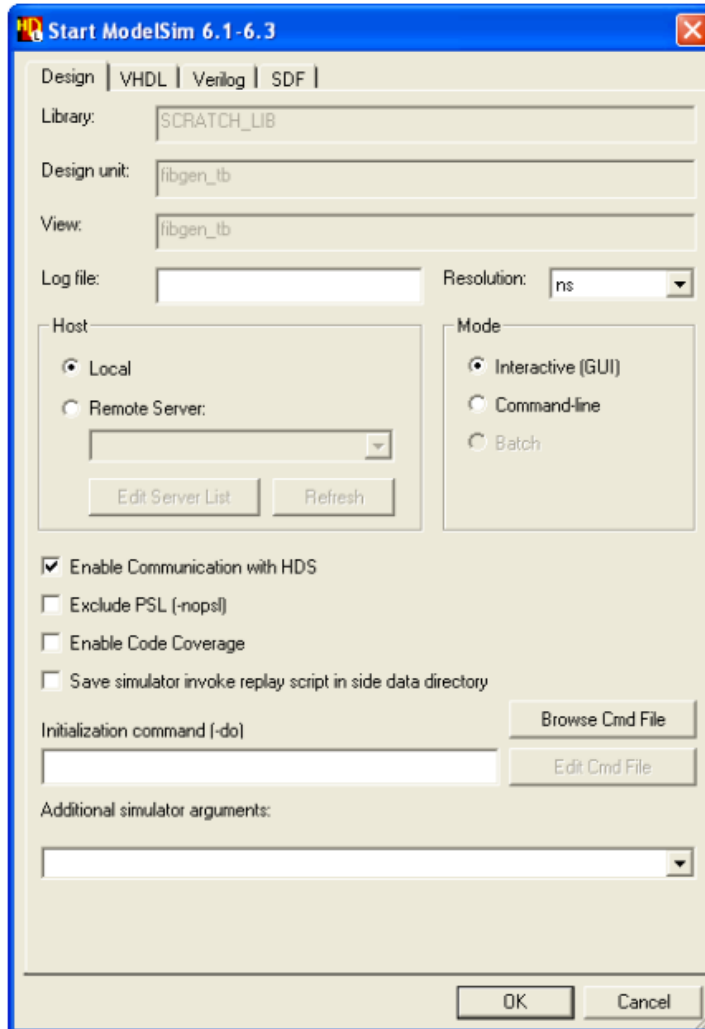
Save test bench



Simulate the design

1. Select the *fibgen_tb* component and use the **ModelSim Flow** button to run the ModelSim flow.

The **Start ModelSim** dialog box is displayed:



Add probes & breakpoints

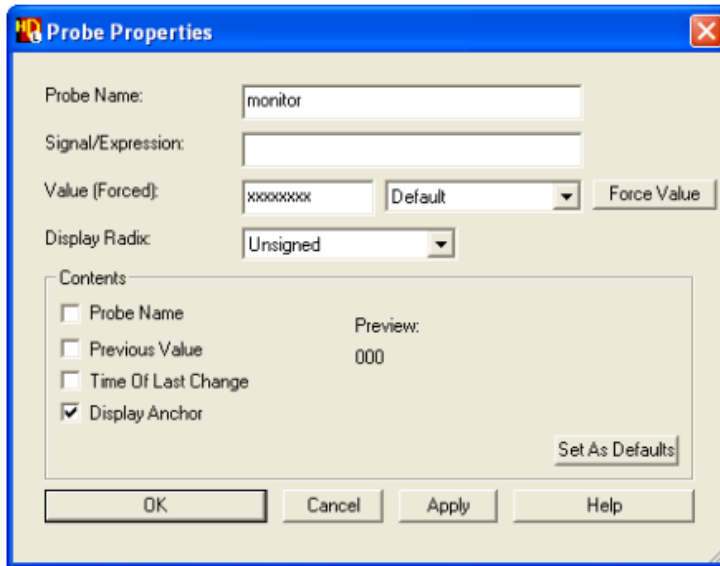
1. Make the *fibgen_tb* block diagram active.

Notice that an additional simulation toolbar is displayed at the bottom of the block diagram when the simulator is invoked. This toolbar provides commands that can be used to control the simulation of the design from the graphical view.

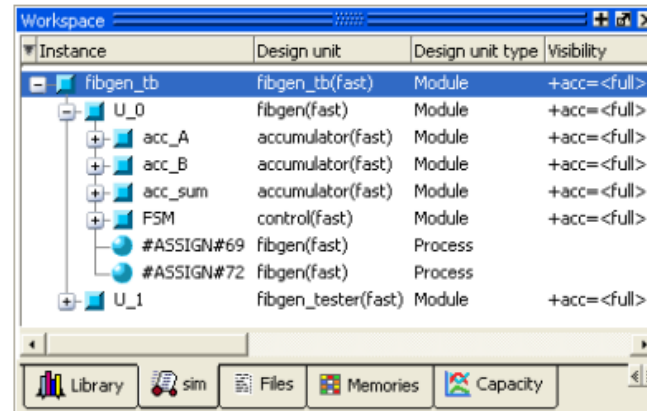
2. Use **Shift + Left Mouse Button** to select the *clock* and *reset* signals and the *monitor* bus of the *fibgen* component.
3. Click the **Add Probe** button in the simulation toolbar to add probes on the diagram which show the current value of each signal.
4. Select the probe on the *monitor* signal and use the right mouse button to choose **Probe Properties** from the popup menu. The **Probe Properties** dialog box is displayed.
5. Choose *Unsigned* from the dropdown list for the *Display Radix* and confirm the dialog box.

```

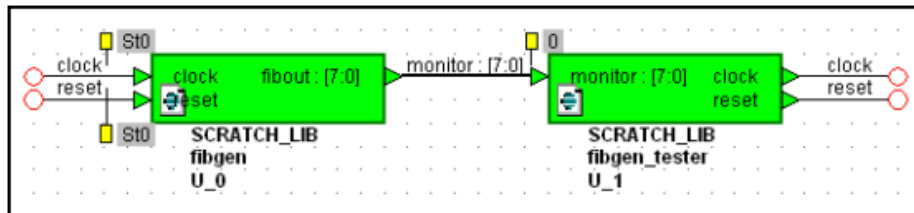
h v81P5/Hds/examples/hds_scratch/scratch_lib/hdl/Seq_Generator.v
Ln#
192      clr_regs: begin
193      clr = 1 ;
194      inc = 0 ;
195      ld_A_B = 0 ;
196      ld_sum = 0 ;
197      end
198      inc_accb: begin
199      clr = 0 ;
200      inc = 1 ;
    
```



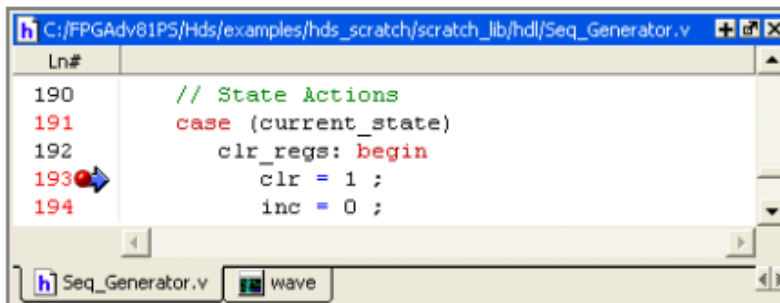
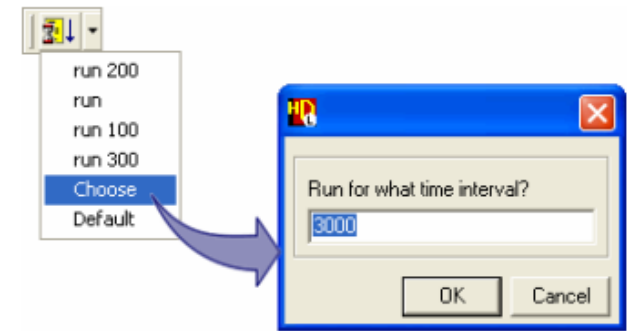
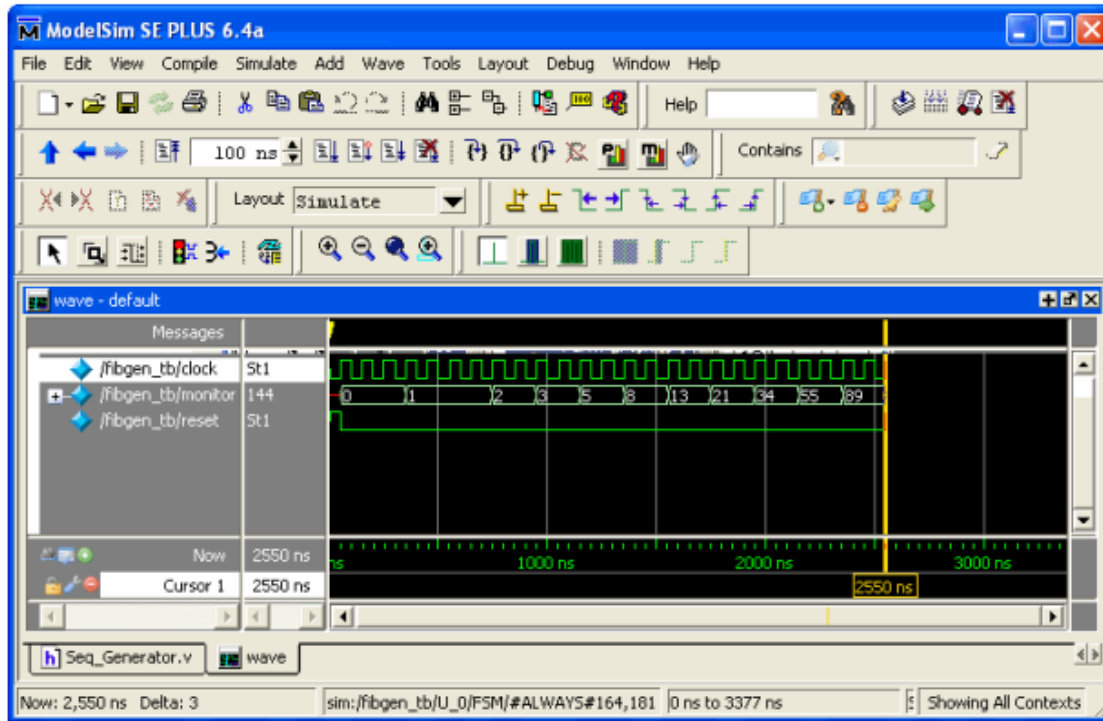
1. Use the icons to expand the hierarchy of the *fibgen_tb* design in the **sim** structure tab of the ModelSim workspace window. Select the *FSM* view under the *U_0* instance if you are using Verilog (or the *fsm* view under the *i0* instance if you are using VHDL).




The block diagram should look similar to the following picture:



Run the simulator

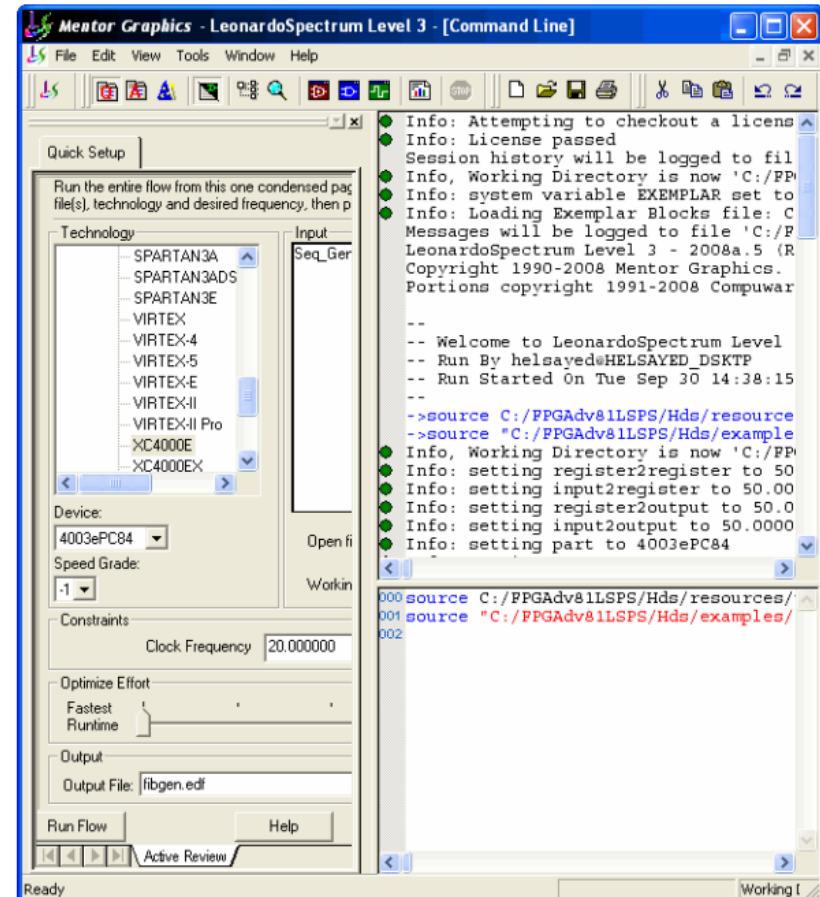
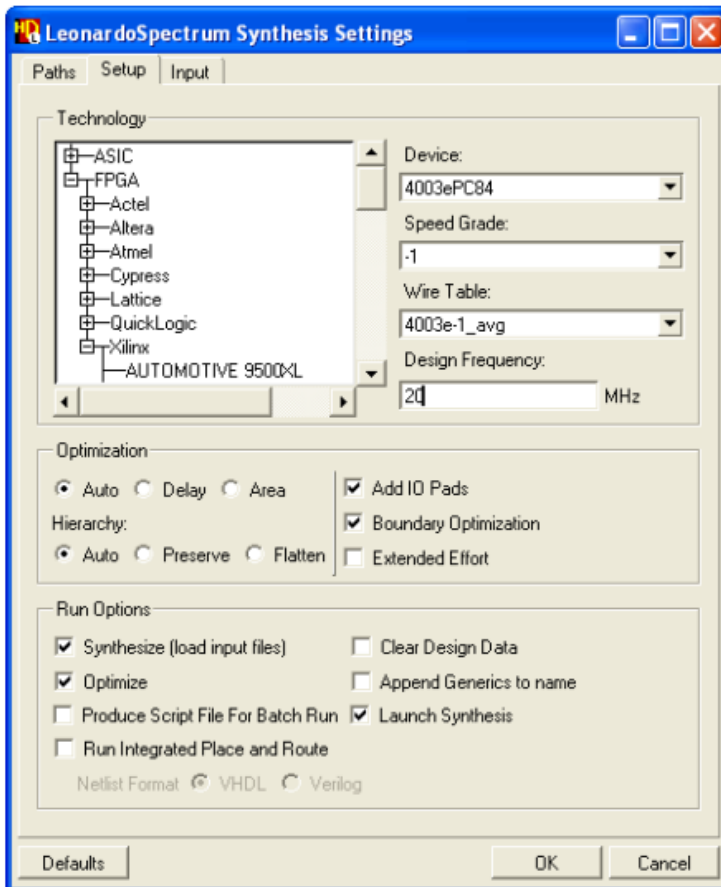


Synthesize the design

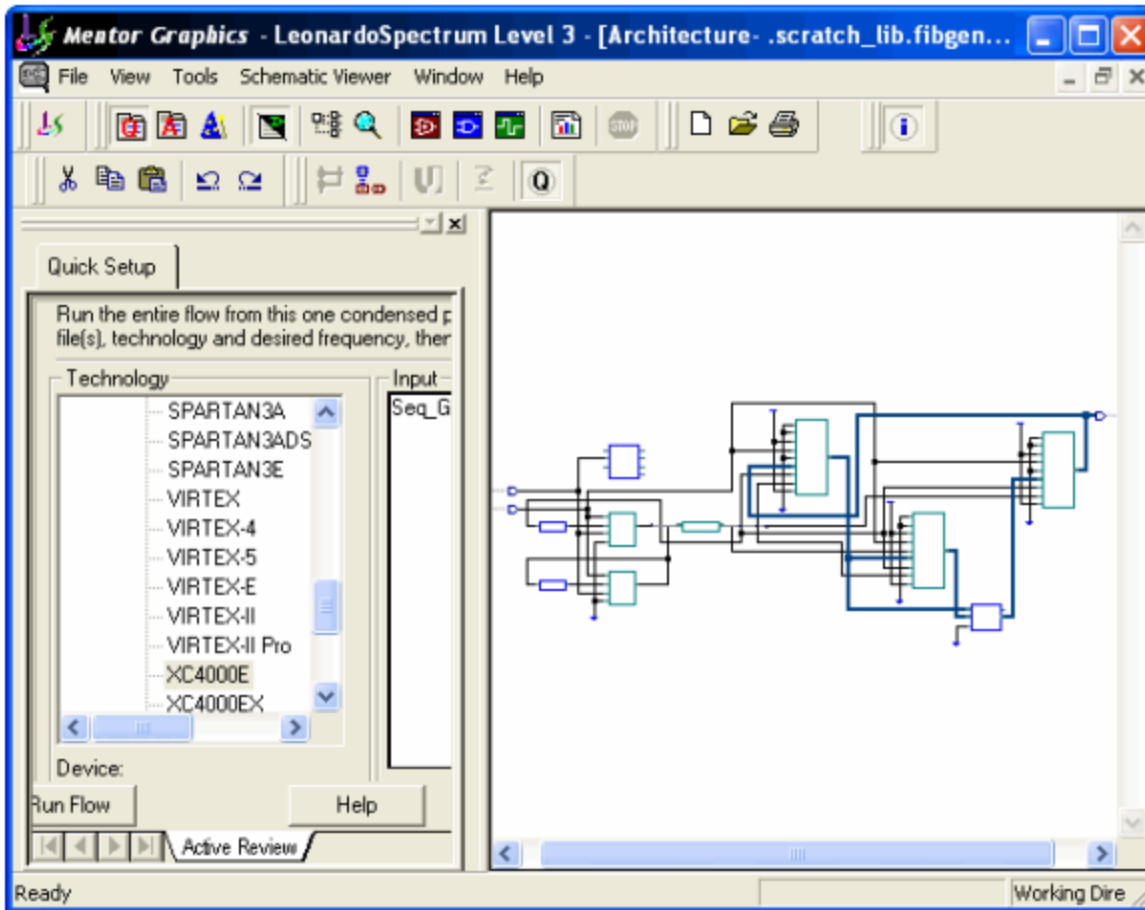
1. Select the *fibgen* component in the design manager and click on the  button. To add the button to the toolbar choose **Toolbar** from the **Add to** cascade of Leonardo Spectrum flow popup menu in the Tasks pane.

The LeonardoSpectrum Synthesis Settings dialog is displayed.

2. Select the technology of your choice in the **Setup** tab. For example, choose *FPGA*>
Xilinx> *XC4000E*.



View RTL Schematic



- For more details, refer to:
 - FPGA Advantage tutorial[®],
http://hornad.fei.tuke.sk/predmety/ncs/FPGA_Advantage_Documentation/getstart.pdf
 - ModelSim tutorial[®],
http://bertrand.granado.free.fr/Sysprog/SysProg/Cours_files/moodelsim_tut.pdf
- The lecture is available online at:
 - <http://bu.edu.eg/staff/ahmad.elbanna-courses>
- For inquiries, send to:
 - ahmad.elbanna@feng.bu.edu.eg