BENHA UNIVERSITY
FACULTY OF ENGINEERING AT SHOUBRA

Post-Graduate

ECE-606

CAD of Electronics

Lecture #3

Design, Simulation and Synthesize Tool Example

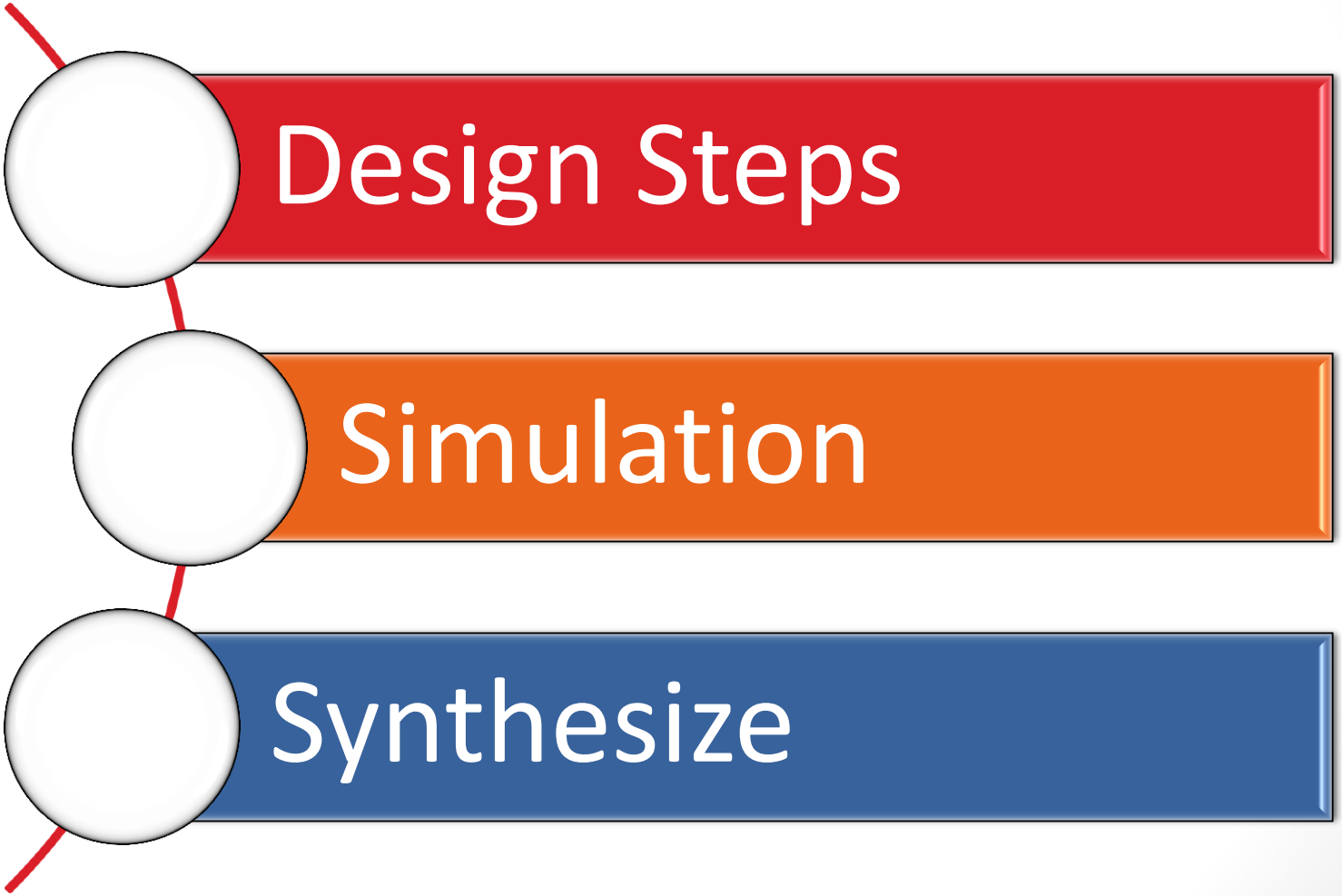
Instructor:

Dr. Ahmad El-Banna

DECEMBER 2014

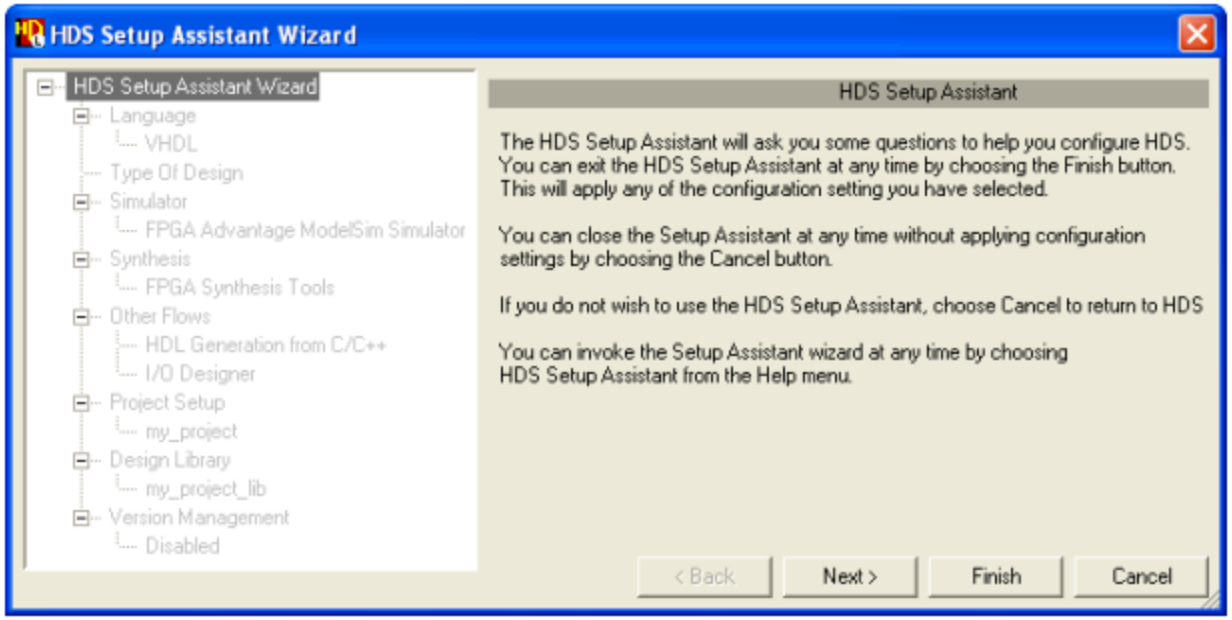
Agenda

Lecture & Lab

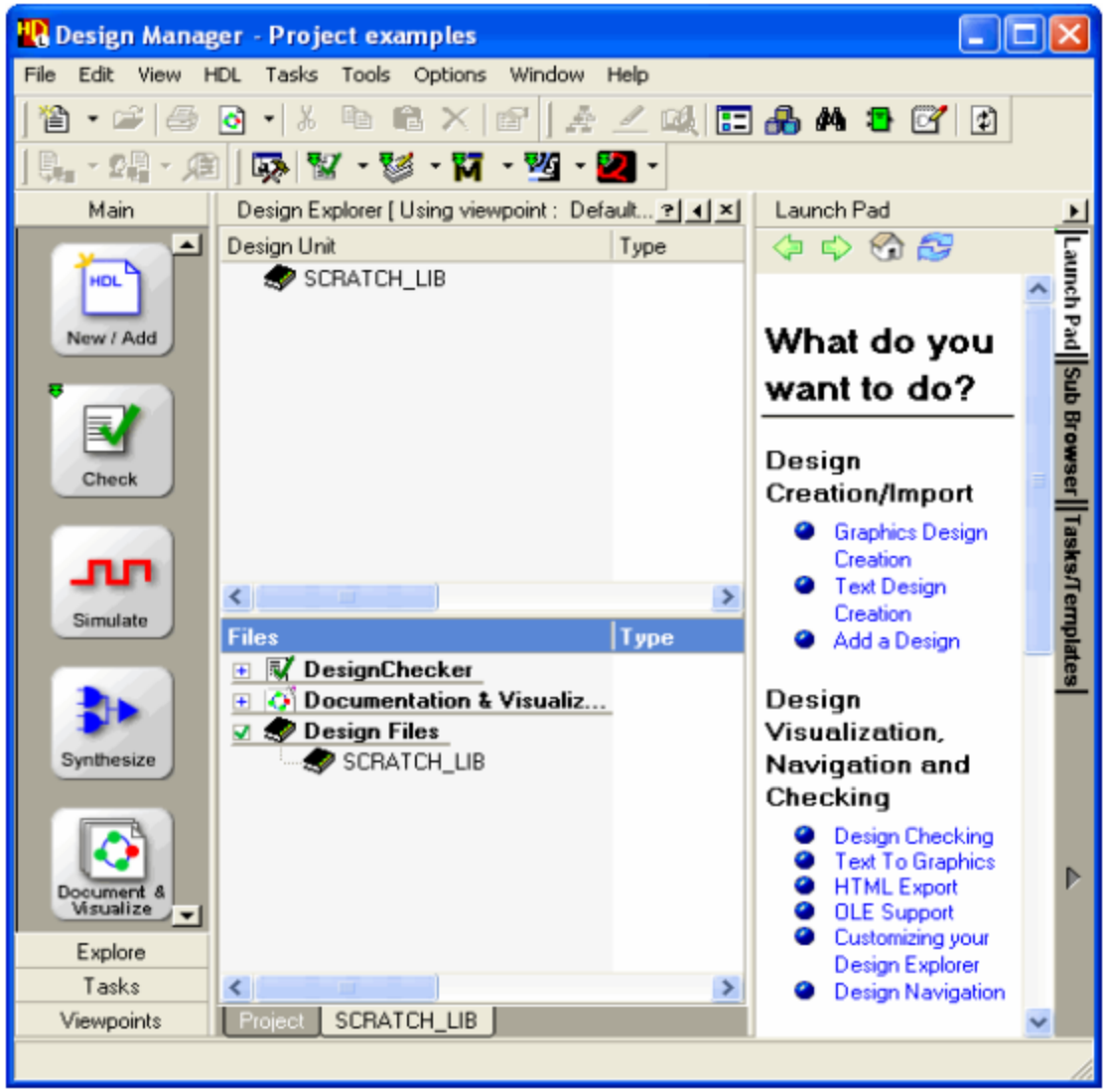


Invoking the Wizard

You can invoke the wizard at any time by choosing **HDS Setup Assistant** from the **Help** menu in the Design Manager window.



The Design Manager

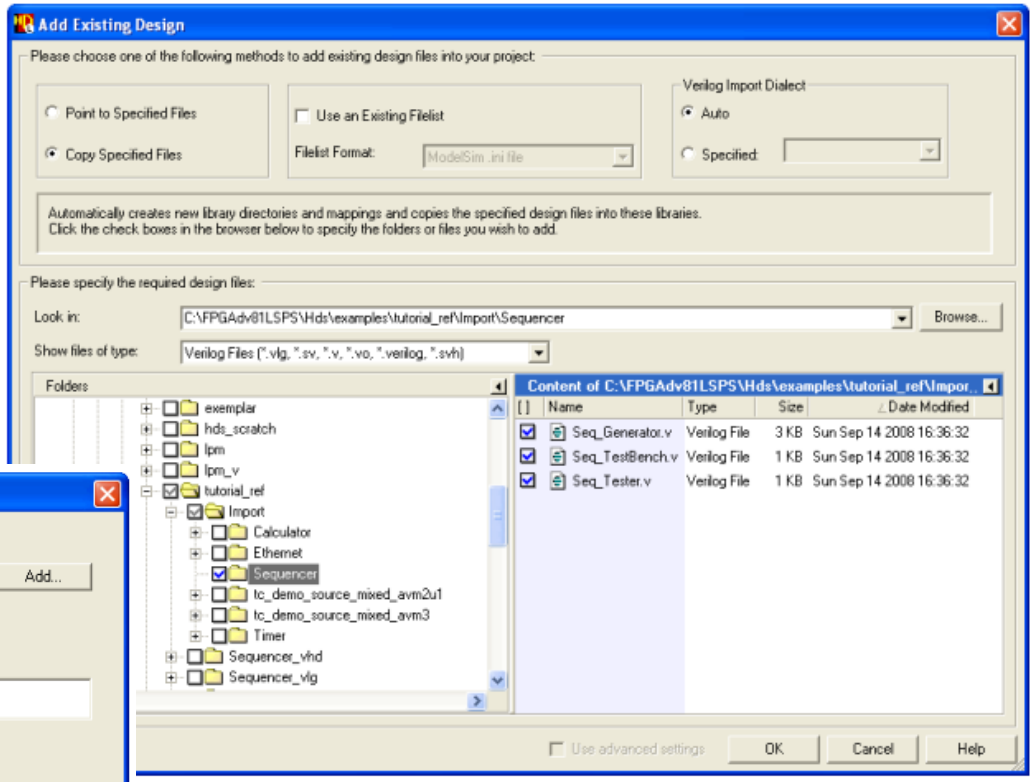


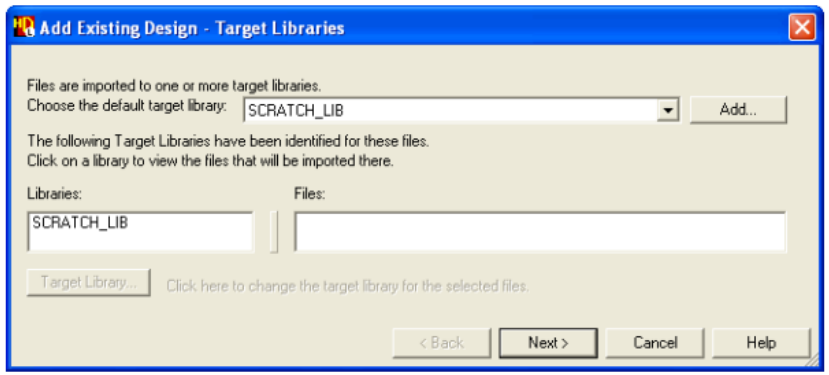
Import Design

1. Choose **File> Add> Existing Design**.
2. Specify the method to add your design by selecting the *Copy Specified Files* option.
3. In the *Folders* pane, browse to the Fibonacci sequencer source code in the *examples* sub-directory of your FPGA Advantage installation. For example, if FPGA Advantage has been installed in the directory *C:\FPGAdv81LSPS*, the path to locate the tutorial source files would be:

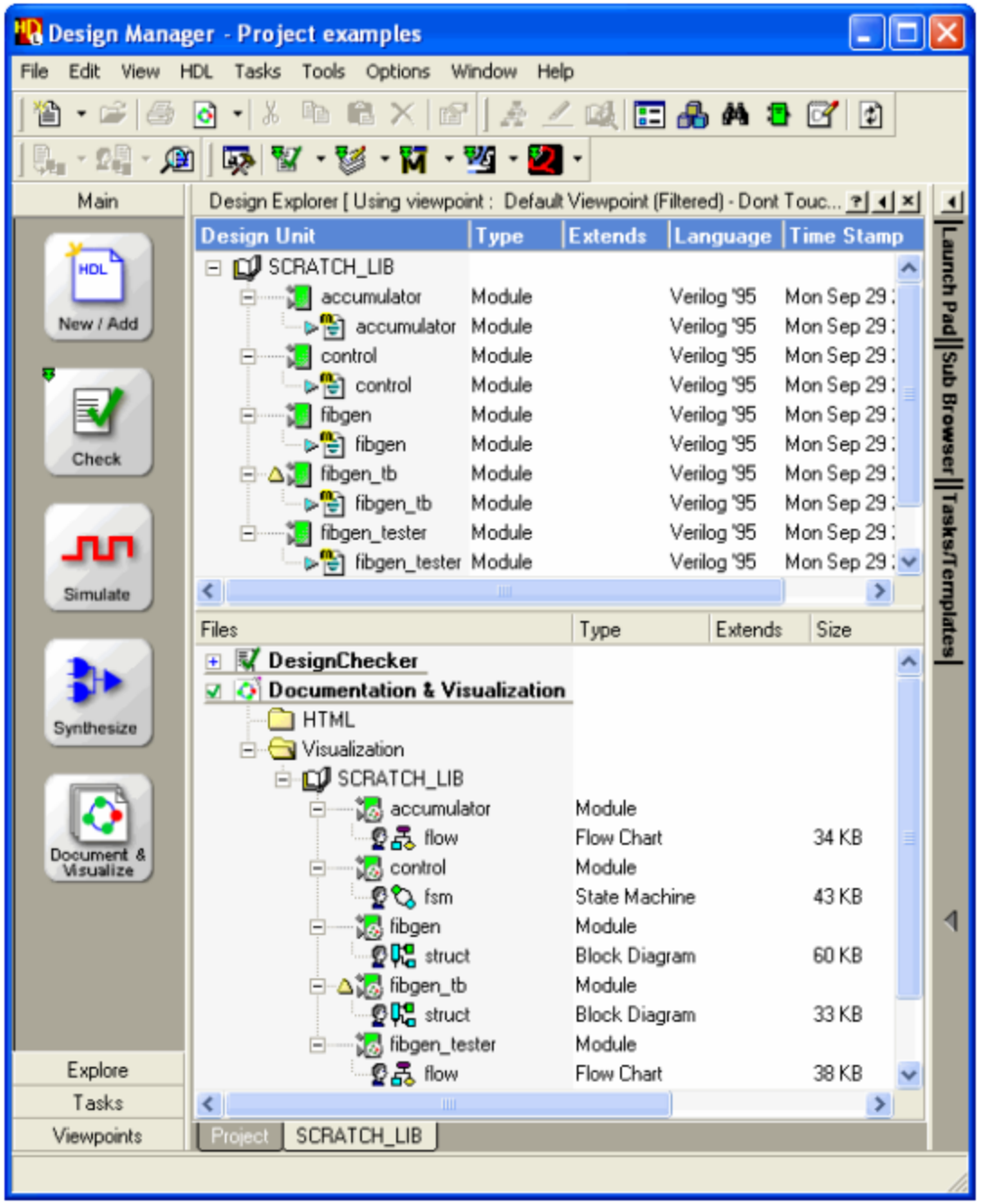
   C:\FPGAdv81LSPS\Hds\examples\tutorial_ref\Import\Sequencer

4. From the *Show files of type* list box select *Verilog Files*.





Browse a design

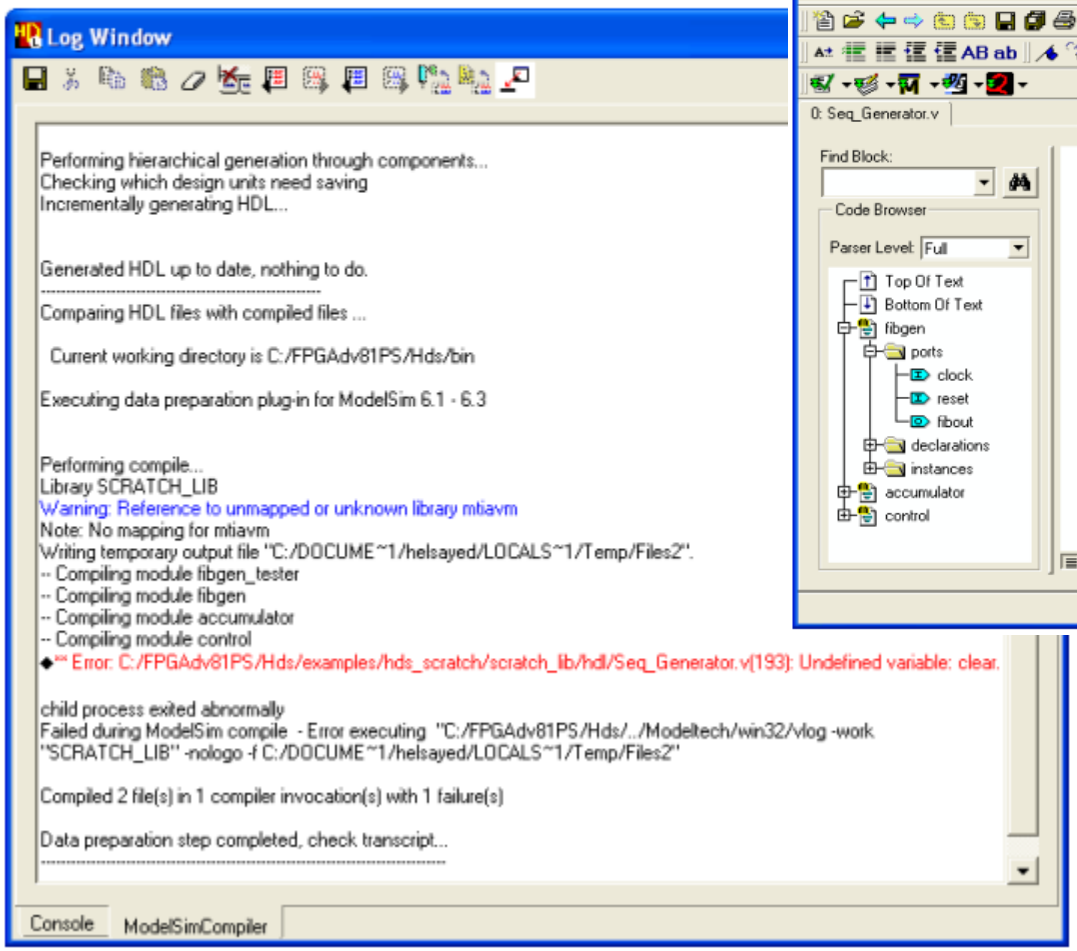


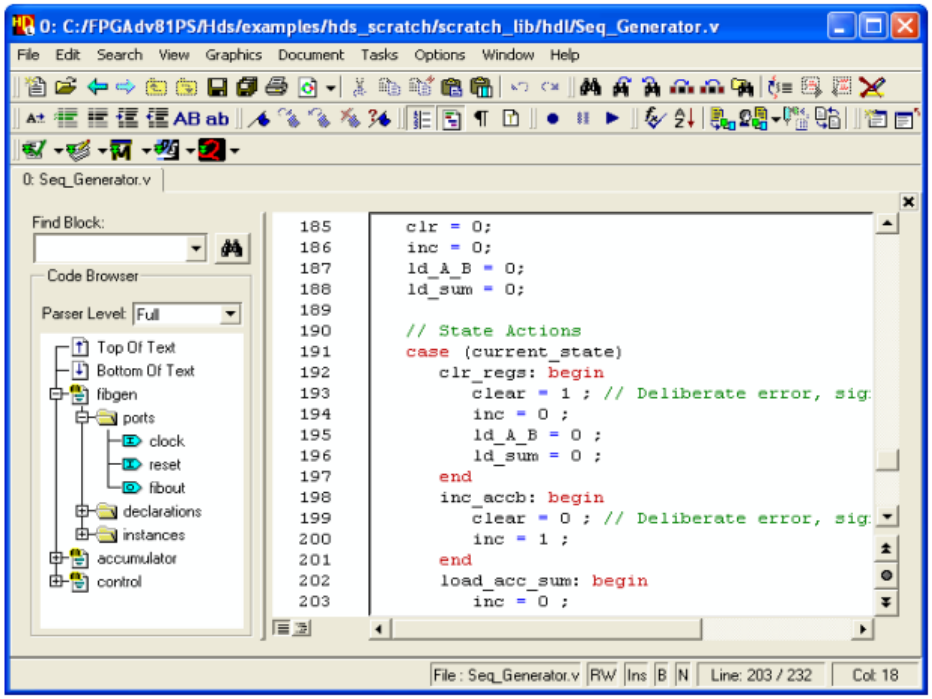
Use Model SIM to debug the design

1. Select the component design unit icon for *fibgen_tb* in the design manager.
2. Click the **Model*Sim* Flow** button in the design manager toolbar.

   FPGA Advantage attempts to run the Model*Sim* flow but HDL compilation fails due to deliberate errors in the design example source code.

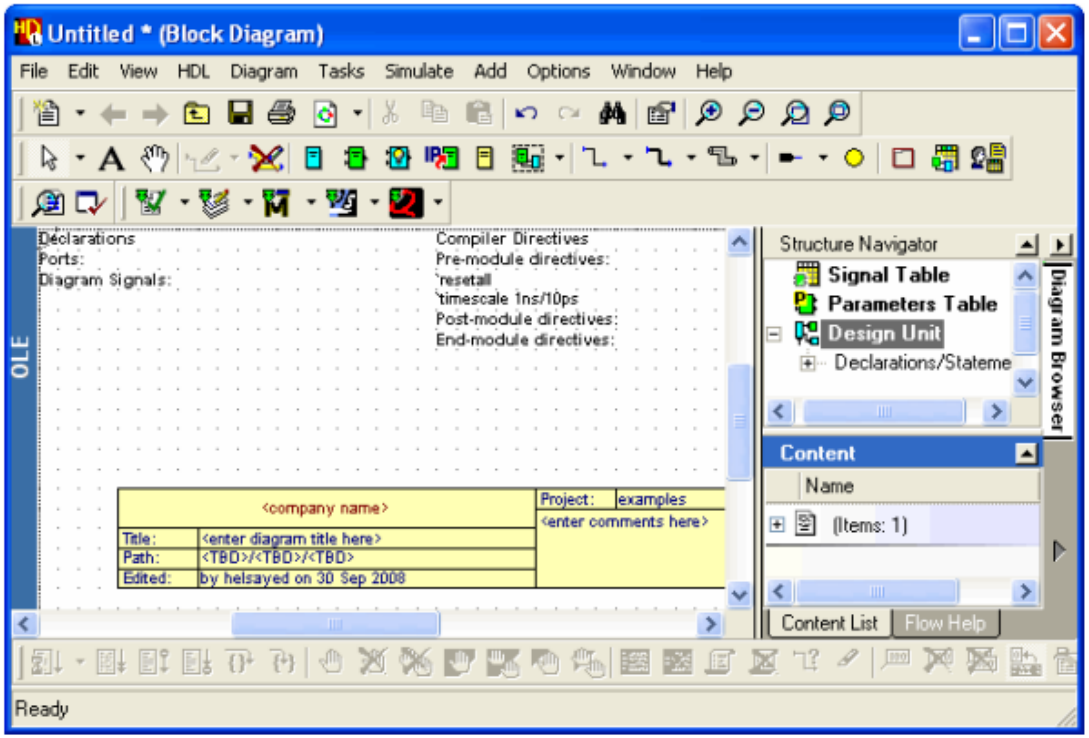
   The compilation status is displayed in the **Log Window**:

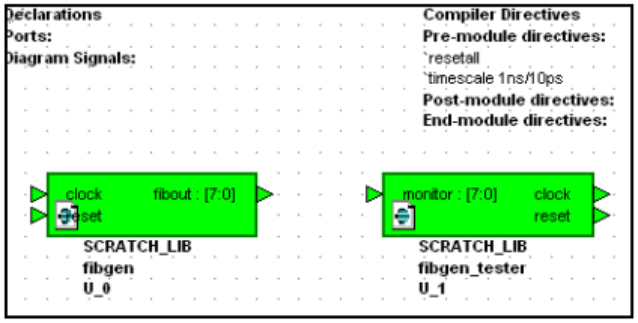




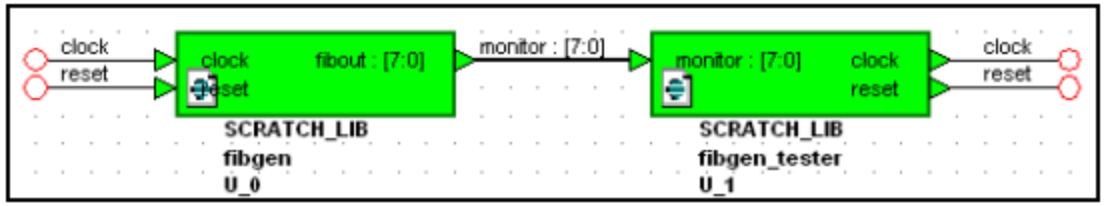
Create a graphical test bench

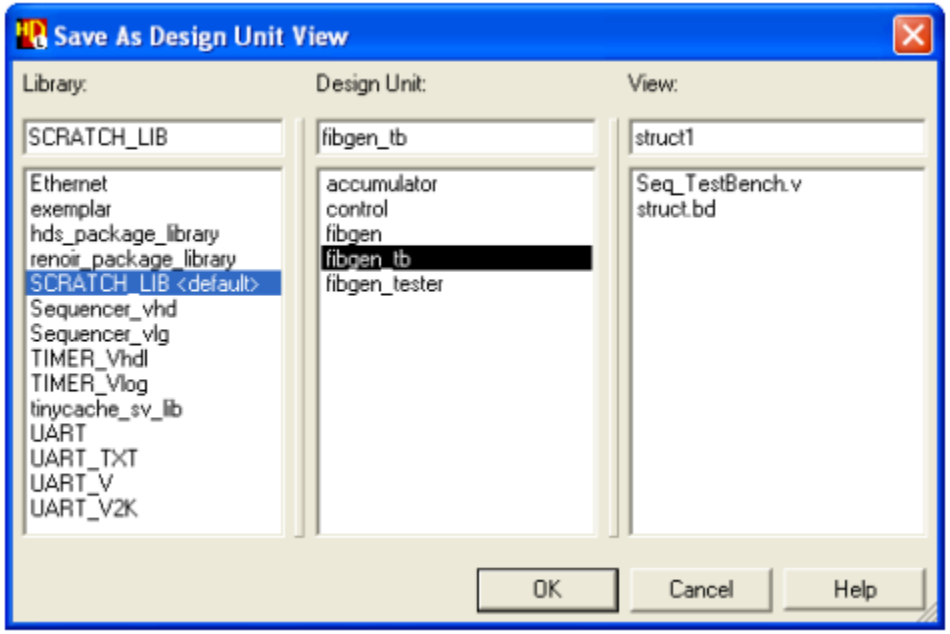
1. Use the **New** button in the design manager window and select **Block Diagram** from the **Graphical View** cascade of the dropdown menu to create a new untitled block diagram.





Save test bench

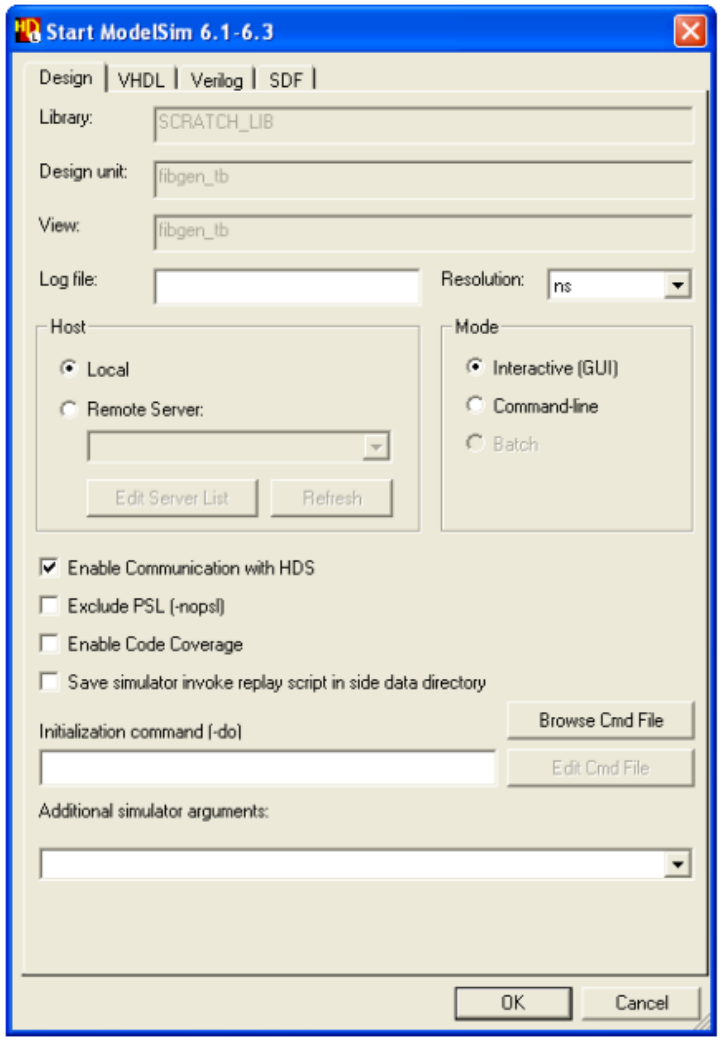


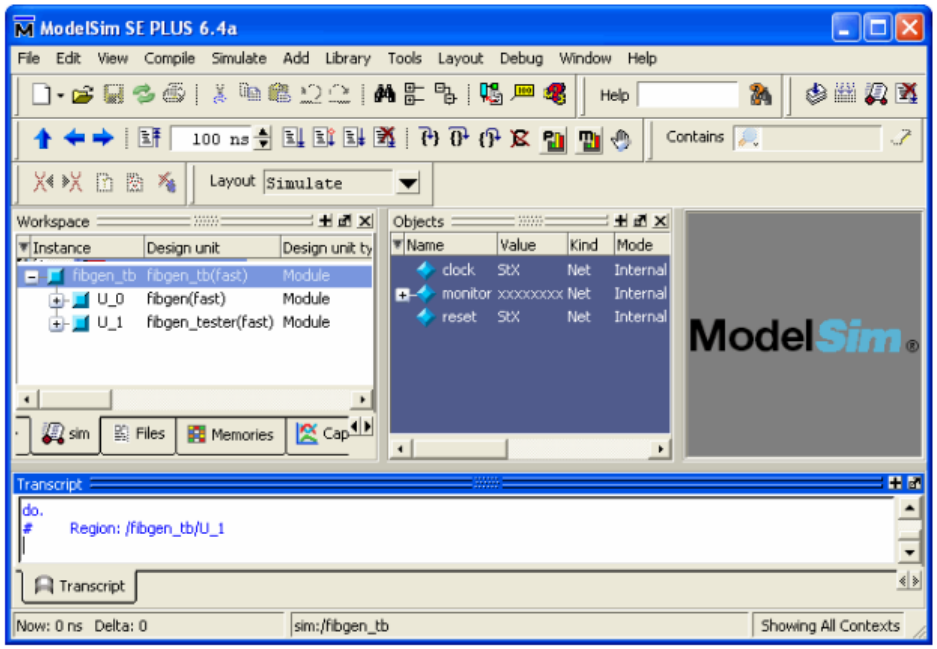


Simulate the design

1. Select the *fibgen_tb* component and use the **ModelSim Flow** button to run the Model*Sim* flow.

   The **Start Model*Sim*** dialog box is displayed:





Add probes & breakpoints

1. Make the *fibgen_tb* block diagram active.

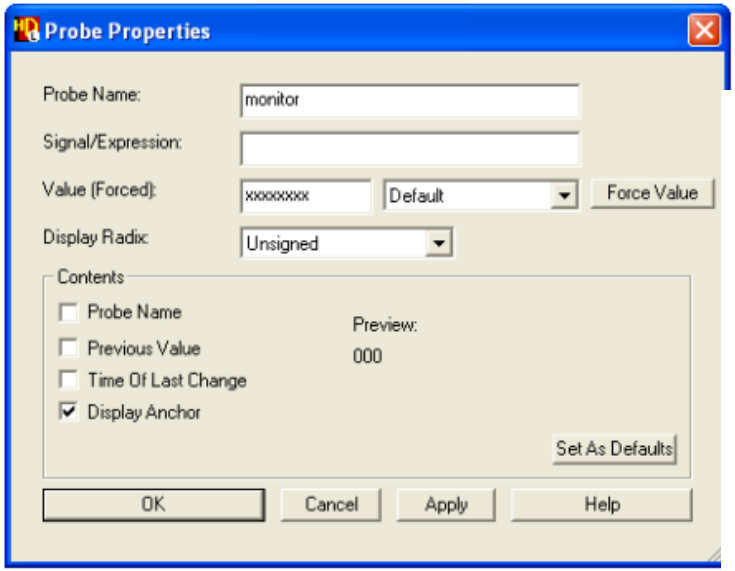
   Notice that an additional simulation toolbar is displayed at the bottom of the block diagram when the simulator is invoked. This toolbar provides commands that can be used to control the simulation of the design from the graphical view.

2. Use **Shift + Left Mouse Button** to select the *clock* and *reset* signals and the *monitor* bus of the fibgen component.

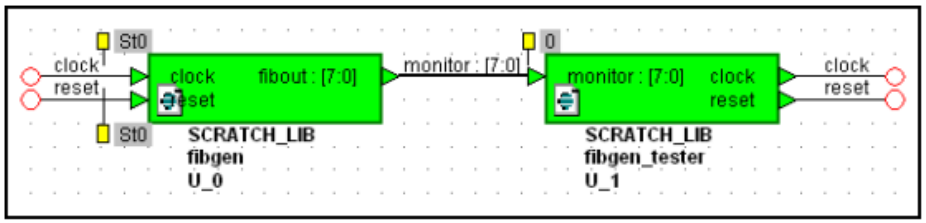
3. Click the **Add Probe** button in the simulation toolbar to add probes on the diagram which show the current value of each signal.

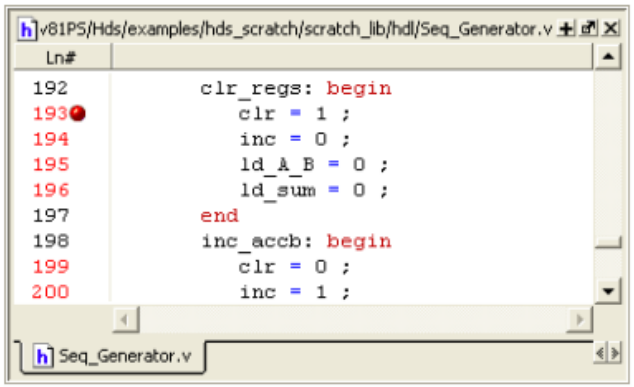
4. Select the probe on the *monitor* signal and use the right mouse button to choose **Probe Properties** from the popup menu. The **Probe Properties** dialog box is displayed.

5. Choose *Unsigned* from the dropdown list for the *Display Radix* and confirm the dialog box.

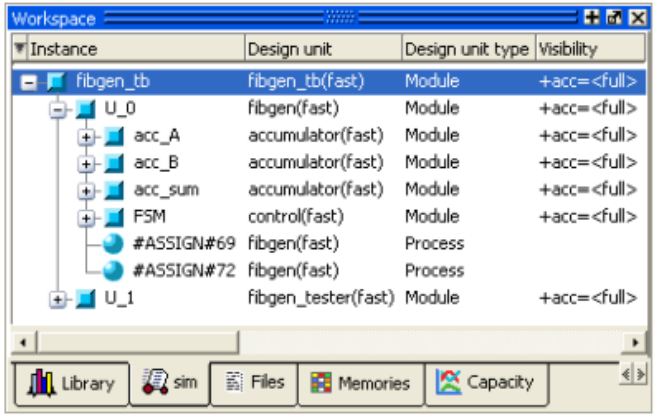


The block diagram should look similar to the following picture:

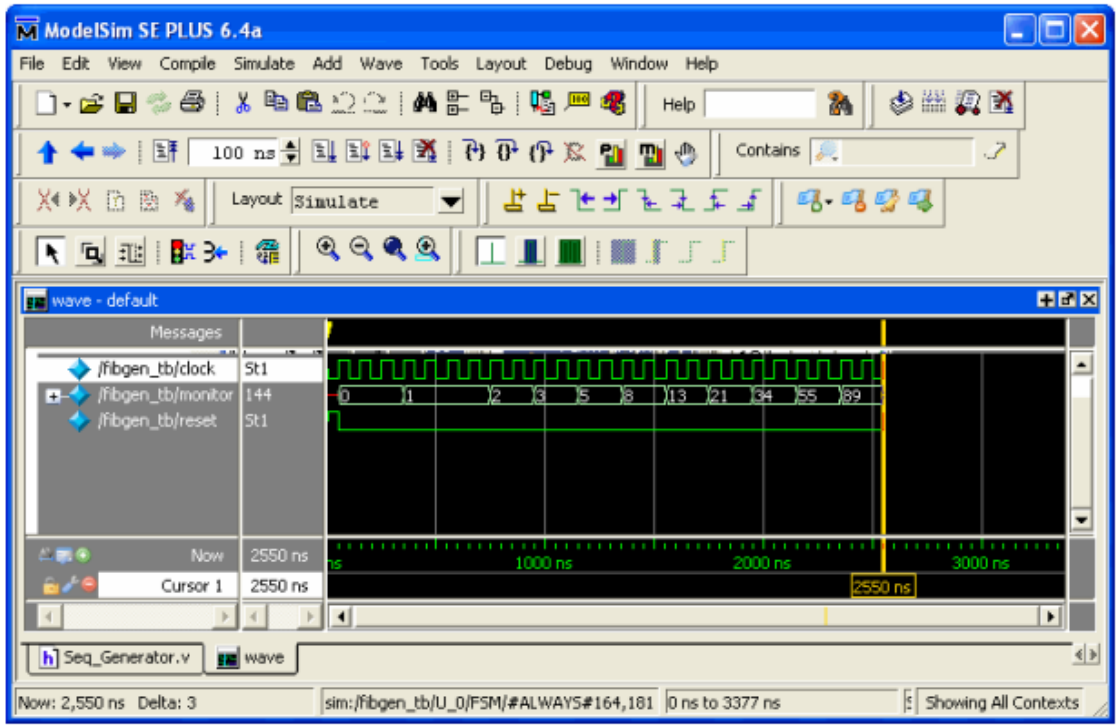


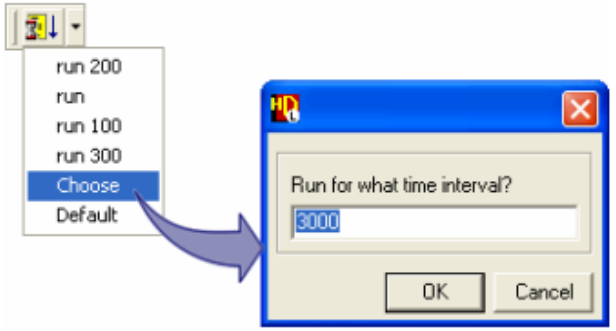


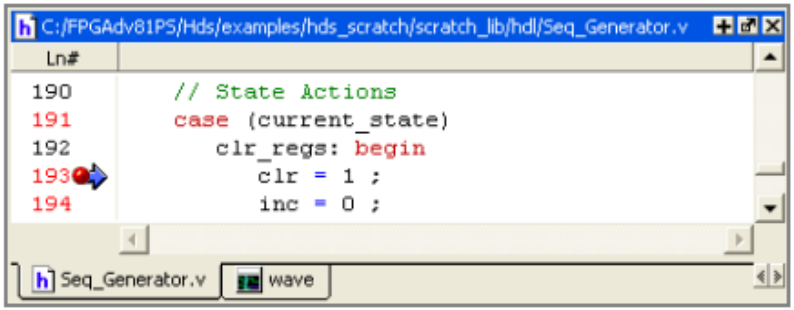
1. Use the ⊞ icons to expand the hierarchy of the *fibgen_tb* design in the **sim** structure tab of the Model*Sim* workspace window. Select the *FSM* view under the *U_O* instance if you are using Verilog (or the *fsm* view under the *i0* instance if you are using VHDL).



Run the simulator





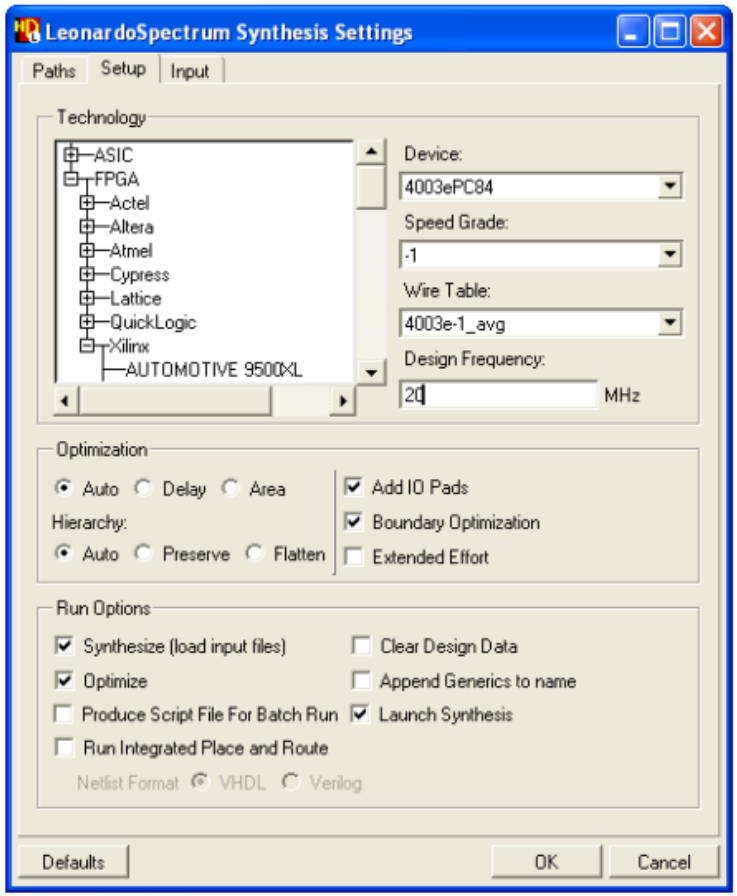


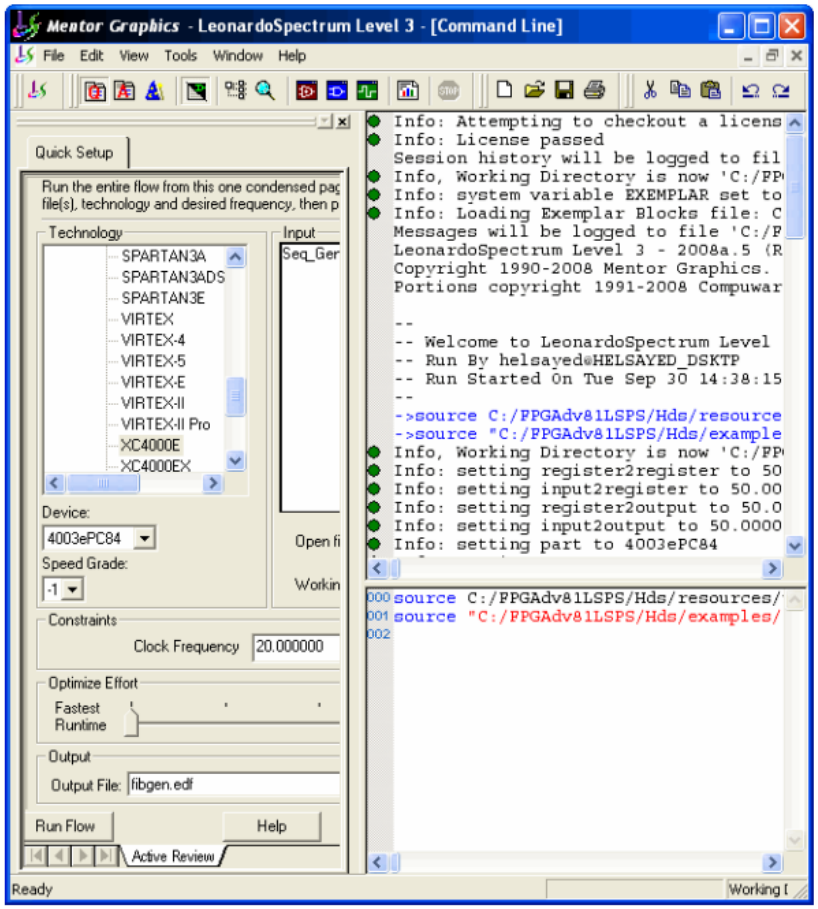
Synthesize the design

1. Select the *fibgen* component in the design manager and click on the  button. To add the button to the toolbar choose **Toolbar** from the **Add to** cascade of Leonardo Spectrum flow popup menu in the Tasks pane.

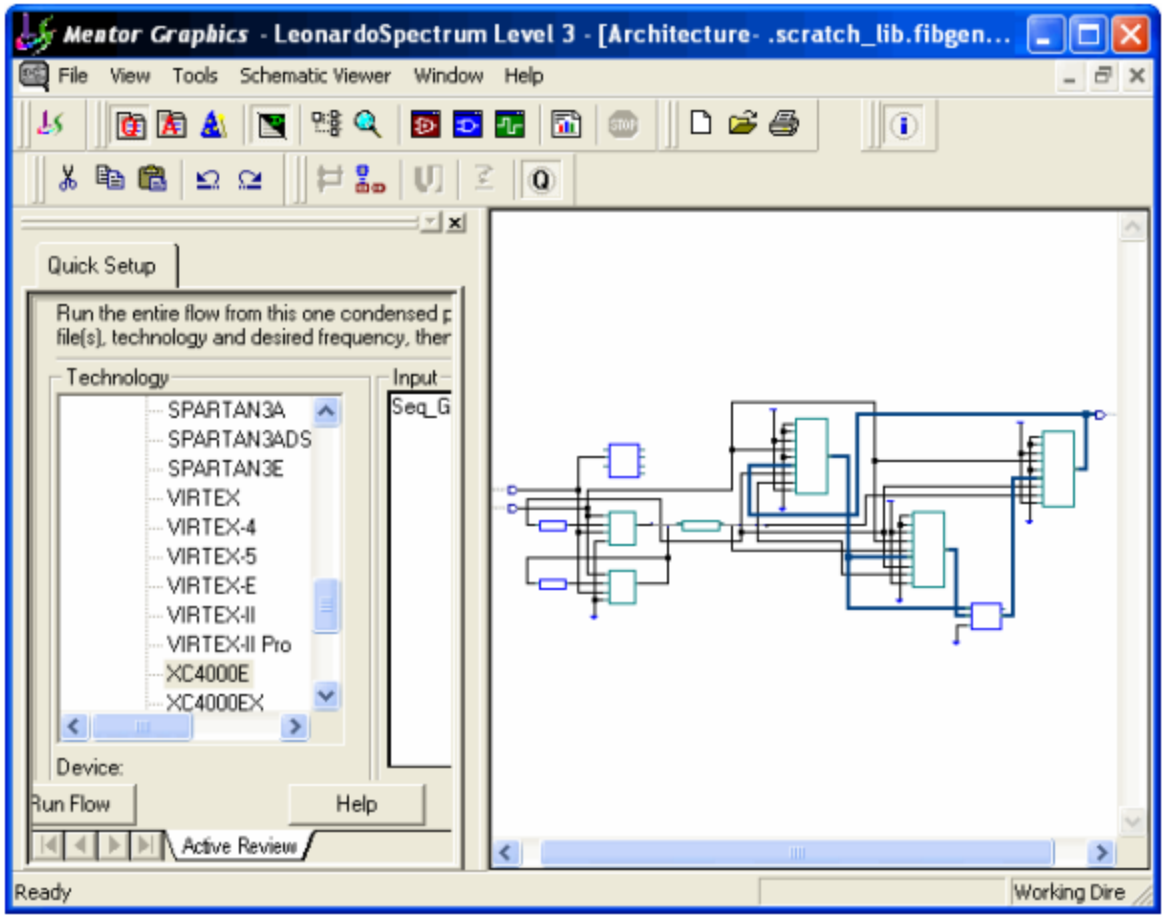
   The LeonardoSpectrum Synthesis Settings dialog is displayed.

2. Select the technology of your choice in the **Setup** tab. For example, choose ***FPGA*> Xilinx> *XC4000E***.





View RTL Schematic



- For more details, refer to:
  - FPGA Advantage tutorial ®, http://hornad.fei.tuke.sk/predmety/ncs/FPGA_Advantage_Documentation/getstart.pdf
  - *ModelSim tutorial ®* , *http://bertrand.granado.free.fr/Sysprog/SysProg/Cours_files/modelsim_tut.pdf*
- The lecture is available online at:
  - *http://bu.edu.eg/staff/ahmad.elbanna-courses*
- For inquires, send to:
  - ahmad.elbanna@feng.bu.edu.eg